REMARKS

This is in response to the Office Action dated October 22, 2007. In that Office Action, at paragraph 2, Examiner indicated that claim 36 would be allowable if rewritten or amended to overcome the rejections(s) under 35USC112, 2nd paragraph, and 35USC101. Claims 3-7 and 9 were also rejected under35 USC112, second paragraph and 35USC 101 (see paragraphs 3 and 4 of the Office Action). It is presumed that claims 3-7 and 9 were rejected because they depend from claim 36, as there was no separate specific objection raised for claims 3-7 and 9.

Claim 36 has been amended and every effort has been made to be responsive to all of Examiner's concerns. Accordingly, amended claim 36, as well as claims 3-7 and 9 are believed to be no longer rejected under 35USC112.

In paragraph 4 of the Office Action, Examiner has raised for the first time a rejection under 35USC101. This comes as a surprise as the invention is clearly not a software program. The recited elements such as: register, detector, filter, shifter and oscillator are clearly hardware items. By way of example, Applicants have enclosed a copy from The Living Webster Encyclopedia Dictionary of the English Language, definitions of filter and oscillator. The definition of "filter" in relevant part states: "an apparatus which controls...electrical currents by checking or lessening certain waves or frequencies without greatly affecting others". The definition of "oscillator" in relevant part states: "a device producing the oscillations which give rise to electric waves". In each case, the definition referred to an "apparatus" or "device" and not a software program. Thus, by way of these exemplary definitions, it is noted that filters and oscillators are, by definition, hardware structures. To the extent that this new ground of rejection (not necessitated by any amendment of the claims) is understood, it is believed to be overcome by the foregoing explanation.

Accordingly, claims 36, 3-7 and 9 are believed to be in condition for allowance. In order to more succinctly set forth their invention, claim 37 dependent from allowable claim 36 has been added as a new claim. Claim 37 is readable, for example, on FIG. 7.

Claim 37 is believed to be allowable not only because it depends from an allowable claim but also because it incorporates additional features (from claim 17).

On page 4, paragraph 4 of the Office Action, Examiner stated: "IDS objections as being missing related application numbers as indication provided by applicant in the specification, paragraph [0001], line 5, see section 1.98". To the extent understood, Applicants respond to this objection by attaching a copy of a portion of an amendment dated January 23, 2006. This document was found by accessing PAIR for this patent application, under TAB for image file wrapper at 01-25-2006 -- Specification. To the extent that this new objection (not necessitated by any amendment of the claims) is understood, it is believed to be overcome by the foregoing explanation.

On page 4, paragraph 5, Examiner notes that the scopes of amended claims 10 and 17 are moot in view of the new grounds of rejection. Regarding claim 10, Applicants reassert the rationale for the patentability of this claim and all claims depending therefrom and hereby incorporate the remarks made in prior amendments herein. An additional amendment (modification of one word) has been made to claim 10 in this amendment for the purpose of enhancing clarity and not for the purpose of changing the scope of claim 10. The remarks regarding claim 10 are similarly applicable to claim 17. Although the currently submitted amendment of claim 17 is more extensive than the amendment of claim 10, the amendment of claim 17 is also submitted for the purpose of enhancing clarity and not for the purpose of changing the scope of claim 17.

On page 4, paragraph 6, Examiner notes that Applicants' arguments filed 7/10/2007 have been fully considered but were not persuasive. In the course of responding (hereinbelow) to the rejections (based in part on newly cited references) in the Office Action dated October 22, 2007, Applicants will further explain the reasons that all the claims should be allowed.

On page 4, paragraph 7, Examiner has cited the case of *In re Gorman,* for the proposition that: "reliance on a large number of references in a rejection does not, without more, weigh against the obviousness of the claimed invention (emphasis

added). Applicants note that even with the large number of references, none of them teach or suggest Applicants' invention either individually or after assemblage in a large group. What the references seem to disclose is some of the same prior art hardware blocks used by Applicants, albeit connected in a different way and without solving the problem solved by Applicants in the manner solved by Applicants.

On page 4, paragraph 8 of the Office Action, Examiner states that: "Regarding applicant's argument to claim 10 with respect to the cited references do not disclose data serialization in a plesiochronous system. In response to applicant's argument it is noted that the features upon which applicant relies (i.e. plesiochronous system) are not recited in the rejected claim(s)." To the extent understood, Applicants respond to this rejection by noting that claim 10, as had been amended, is directed to: "10 In a plesiochronous system, a method for PLL/DLL data serialization comprising:" (emphasis added). Accordingly, it is requested that this rejection be withdrawn.

On page 5, paragraph 9, Examiner argues that Gu and Song may be legitimately combined to make a case of obviousness. In response, Applicants restate their prior position and also that, *arguendo*, even if properly combined, the combination does not teach or suggest the invention of Applicants. The fact that Gu does not relate to a plesiochronous system, does not relate to a transmitter/serializer, does not address the problem addressed and solved by Applicants and other important distinctions are serious short-comings in Gu that go far beyond Examiner's characterizing Gu's shortcomings simply as: "connection between a FIFO register with a phase detector".

Moreover, Examiner's reliance on the fact that :"both of the cited references relate to the same environment: e.g. data synchronization system" is misplaced as it is an oversimplification. The fact that Song relies on bit stuffing (a technique avoided by Applicants) has been previously noted. It is respectfully urged that combining the teachings of Gu (related to an asynchronous receiver and not suggesting a FIFO), with the Song patent (related to bit stuffing) is not an obvious combination and even if combined would not obviously result in a plesiochronous transmitter/serializer that overcomes the problems associated with bit stuffing by completely avoiding bit stuffing. Also, the fact that important recitations in Applicants claims directed to the particular

connection of the FIFO register are suggested by neither Gu nor Song result in the fact that neither Gu nor Song cover the invention claimed by Applicants.

On page 5, paragraph 10, regarding claim 17, Examiner notes that "transmitting from a none-secure to secure system" is not present in claim 17 and therefore cannot be read into the claim as a limitation. Applicants agree. Nevertheless, Applicants continue to assert that the combination and coaction of structural elements as recited in claim 17 are novel, unobvious and useful. The fact that a particular utility or result that is achievable with the invention is not specifically recited in claim 17 does not detract from its patentable import.

Beginning on page 6 of the Office Action, Examiner describes the claim rejections under 35USC103 in greater detail than before. In these rejections, Examiner introduces the Wu US patent 6,329,859 and Momtaz US patent 5,950,115 as brand new references and applies the previously cited references, as well, partially in a new and different way. Examiner's collection of references is certainly thorough and helpful. Accordingly, Applicants are required to take this, as their first opportunity, to respond and point out how all of these references fail at the point of novelty and therefore confirm the patentable import of this invention.

Claims 10-11 are rejected as being unpatentable over Wu, in view of Gu, Filip, Schatz and Momtaz.

Regarding Wu, it is agreed that Wu teaches an N-way circular phase interpolator for generating a signal having arbitrary phase. In the Wu patent, at column 1 lines 1-40, Wu discusses some prior art that is similar to, but not as relevant as the AAPA in FIGs. 1-4 of Applicants' specification. In this regard Wu specifically mentions "plesiochronous clocks" and notes that these cannot be generated by using DLL's. By suggesting this incompatibility between plesiochronous clocks and DLL's, it is clear that the Wu patent teaches away from Applicants' invention rather than suggesting Applicants' invention. Neither the hardware parts nor the method recited in Applicants' claims can be found in Wu. In order to highlight the novel and unobvious aspects of claim 10, it is here reproduced, as follows:

10. (Currently amended) In a plesiochronous system, a method for PLL/DLL data serialization comprising:

detecting a local reference at a phase/frequency detector (PFD) of a phase lock loop (PLL);

phase locking a voltage controlled oscillator (VCO) of said PLL to a local reference to suppress a phase noise of said VCO;

receiving a parallel data input and a data clock at a FIFO register;

filtering, at a delayed lock loop (DLL), a signal representative of a fill level of said FIFO;

phase shifting an output of said VCO of said PLL in response to said filtering step;

locking said PLL to a frequency corresponding to a pre-filtered signal input to said DLL;

receiving, at a parallel-in serial-out (PISO) serializer, said parallel data and said VCO output; and

outputting a serialized data from said PISO serializer with said VCO ~~output~~ outputting a transmit clock. (the underlined word was modified in the current amendment)

None of these method steps can be found in Wu. Regarding Gu, the preamble recited in Applicants' claim 10 is neither suggested nor taught by Gu. Gu's patent relates to a receiver in asynchronous data transmission and does not relate to plesiochronous transmission. As is well known, the majority of data transmission systems are asynchronous. In asynchronous transmission systems, the data rate of a link does not affect the entire system. Also, since Gu's receiver uses a dual loop in a receiver (not transmitter/serializer), he does not have to be concerned about the spectral purity of his received clock and he does not have to address (or solve) problems unique to plesiochronous systems. Applicants claim does not purport to broadly cover the use of dual loops and Gu's teaching does not suggest the combination of claim 10.

Claim 10 recites: "receiving a parallel data input and a data clock at a FIFO register; "

During the prosecution of this application, it has been consistently recognized that Gu has no FIFO register and therefore cannot receive a parallel data input at a FIFO register. However, Gu does receive input data at data recovery 40. However, if one were to substitute a FIFO register for data recovery 40, it would still not receive a parallel data input but rather, a serial data input. (See Gu column 12 lines 25-27 stating: "said data recovery block deserializing the received time division multiplexed data signal". Thus, the input data to Gu's data recovery block 40 cannot be a parallel data input.

Claim 10 recites: "filtering, at a delayed lock loop (DLL), a signal representative of a fill level of said FIFO"

Not only does Gu not have a FIFO but Gu also lacks a signal representative of a fill level of a FIFO. (It is understood that Examiner contends that FIFO's are well known, as for example in Schatz US 6,744,787. Applicants do not disagree with the statement that FIFO's are well known. It is also understood that Examiner contends that with a combination of these 2 patent references, as well as others, Applicants' claimed invention becomes obvious under 35USC 103.) Notwithstanding this latter contention, it continues to be Applicants' position that since none of these other references addressed or solved the same problem as Applicants, there is no rationale or suggestion for how a FIFO would be combined and used with Gu's teaching to address and solve the problem addressed and solved by Applicants. In contradistinction to all of the cited references, Applicants disclose and claim for the first time a combination of structural elements, their functional caction, and method steps reciting HOW a FIFO register can be utilized in a plesiochronous system without the use of stuff bits.

Claim 10 also recites: "outputting a serialized data from said PISO serializer with said VCO outputting a transmit clock"

Gu has no PISO serializer and does not teach outputting serialized data (probably because his disclosure focuses on a receiver and not a transmitter). (It is understood

that Examiner contends that PISO serializers are well known and that this knowledge, as confirmed, for example in Schatz US 6,744,787, includes coupling a FIFO to a PISO. Applicants do not disagree. It is also understood that Examiner contends that with a combination of these 2 patent references, as well as others, Applicants' claimed invention becomes obvious under 35USC 103.) Notwithstanding this last contention, it continues to be Applicants' position that since none of these other references addressed or solved the same problem as Applicants, there is no rationale or suggestion for how a FIFO and PISO would be combined and used with Gu's teaching to address and solve the problem addressed and solved by Applicants. In this regard, note that in Figure 1 of Schatz, parallel to serial converter 18 transmits both Transmit Data and Transmit Clock. In contradistinction, claim 10 recites that the VCO outputs the transmit clock. In other words, the Schatz patent actually teaches away from Applicants' invention by disclosing a transmit clock connection that is different from that of Applicants. This is one more structural and functional distinction of Applicants' invention over the known prior art, Very significantly, the Schatz patent relates to problems with fill data; while Applicants' invention specifically avoids the problems of fill data by avoiding the use of fill data

Examiner cites the Filip patent as disclosing: correlations of executions between phase detectors with phase shifter and VCO. However, the addition of this general knowledge to the other cited references would not have taught one skilled in the art, at the time the invention was made, how to arrive at Applicants' invention. Moreover, Filip discloses a lock detector and does not disclose a phase shifter. For all of the foregoing reasons, claim 10 is believed to recite a patentable invention.

Claims 11-15 depend from claim 10 and are believed to be allowable for the same reasons. Regarding claims 12-13, Examiner added a newly cited reference, to wit, Momtaz. A review of the Momtaz patent reveals that it relates to quickly acquiring lock on a receiver PLL by multiplexing the phase detector on the receiver between a reference clock and the received data stream. In Momtaz at column 1 lines 25, as cited by Examiner and "to incorporate Momtaz's ideas of triggering locks to nominal values" into other ones of the cited references (Wu-Gu-Filip-Schatz noted at page 9, line10 of

the Office Action) would still not achieve what Applicants have invented. Examiner then continuing on page 9, line 10 and the line 11 adds Momtaz and mentions the system "to insure synchronization process without re-initialization and reducing transmission delay". If this prior art recitation could substitute: without the use of stuff bits, then these references might require further explanation. Since the references ignore this important aspect of Applicants' invention, the combination of all these references is clearly not a valid teaching of Applicants' invention.

Examiner has rejected claims 17-18, 23-35 as being unpatentable over Gu, in view of Filip in view of Rotzoll in view of Schmid and further in view of Schatz. This rejection is surprising, as claim 17, (readable on FIG. 7, for example) not only includes the structure and function of a dual loop serializer (as illustrated in FIG. 5, for example), but also recites additional structure and function to form a Dual Loop Retimer. It is Examiner's contention that (somehow)," it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Schmid's ideas of interoperating executions of SIPO shift register, PISO shift register with Gu, Filip, Rotzoll's system in order to be able to transmit a data stream from non-secure channels to secure channels". Examiner specifically refers to Schmid column 9, lines 30-35 and Schatz column 3 lines 1-56. Schatz was previously distinguished hereinabove. Regarding Schmid, Examiner has specifically referenced column 9 lines 30-33. It is agreed that Schmid there discusses secure and non-secure systems. But the notion that this statement is in any way suggestive of Applicants' invention is respectfully traversed.

The newly cited Rotzoll patent relates to a highly integrated television tuner on a single microcircuit. According to Examiner, at column 11, lines 1-20, it discloses a DLL that includes phase detector, phase shifter and filter. Actually, these appear to be audio devices and their existence does not appear to raise a question of obviousness with respect to Applicants' invention. It is hard to imagine how one skilled in the art at the time the invention was made would have gone to this specification and the corresponding drawing figure to solving a problem in plesiochronous data transmission.

Claim 17 succinctly recites:

A plesiochronous data retimer comprising:

a digital delay lock loop (DDLL) receiving an input data to be retimed and configured to recover a clock of said input data;

a phase/frequency detector (PFD) receiving a local reference;

a phase shifter configured in a feedback loop with said PFD;

a first loop filter coupled to said phase shifter;

said phase/frequency detector (PFD), phase shifter and first loop filter forming phase locked loop,

a serial-in and parallel-out (SIPO) deserializer coupled to said input data;

a first-in first-out FIFO register coupled to said deserializer; and

a parallel-in serial-out (PISO) serializer receiving said deserialized input data and transmitting a serialized data.

All the rationale provided for the allowance of claim 10 applies to the allowance of claim17. Claims 18-21 depend from claim 17 and are believed to be allowable for the same reasons. Regarding claims 23-35, rejections have been based on the same rationale and prior art as applied to the other claims. Nevertheless, Applicants note again some specific reasons for the allowability of claims 23-25. For Examiner's convenience, claim 23 is here reproduced, as follows:

23. (Previously presented) A plesiochronous data retiming method comprising:

recovering a clock from a received serial input data at a digital delay locked loop (DDLL);

deserializing said serial data to a parallel data using said recovered clock;

writing said parallel data to a FIFO (first-in first-out);

synthesizing a transmit clock;

reading said parallel data from said FIFO;

serializing said parallel data using said synthesized transmit clock;

detecting a FIFO fill level at a delay locked loop (DLL); and

phase shifting, in a phase lock loop (PLL), an output of a VCO, wherein said phase shifting is in response to said detecting step.

Without repeating specific references to all the claim clauses relating to FIFO (which are absent from Gu), Applicants further note that, as this claim relates to plesiochronous systems, there is no suggestion anywhere in the prior art of:

"synthesizing a transmit clock"; in the manner taught by Applicants in the overall combination, and there is also no teaching of:

"serializing said parallel data using said synthesized transmit clock" in the manner taught by Applicants in the overall combination.

Furthermore, Applicants responses to the same prior art with respect to the prior claims should also be applied towards justifying the allowance of claims 23-35.

In conclusion, it is noted that none of the cited references address or solve the problems solved by Applicants' invention. Moreover, none of the cited references disclose the combination of structural elements, their coaction, function and unexpected result as claimed by Applicants. Applicants' acknowledge only that the numerous cited references collectively establish a bill of materials that includes the building blocks used in the instant invention. However, none of those references either individually or in combination suggest that a plesiochronous data transmission system can achieve what Applicants have done without bit stuffing.

Briefly, Applicants' combination uses the fill rate of a FIFO register and a phase detector to adjust a transmit rate. The transmit rate is adjusted by changing a variable delay after an oscillator. The oscillator is controlled by a PLL. The delay is controlled by a DLL. Although, as was previously noted, oscillators, PLL's, DLL's, as well as other building blocks were previously known, they were never combined as Applicants have done in order to provide a clean transmit rate without having to modify the data rate by using fill data.

Applicants observed that in a plesiochronous system, it was a problem to transmit data that arrives at a slightly different rate than the clean frequency reference they were required to use. They also observed that the transmit data had to be cleaned up in order to make sure that frequency noise (jitter) did not get propagated by the system. They then proceeded to address and solve these problems in a novel and unobvious way.

As previously noted, Gu neither addressed nor needed to solve the plesiochronous data spectral purity problem. Gu's receiver uses a dual loop, but it is not concerned with the spectral purity of the received clock. For this reason, the structural and functional distinctions highlighted in Applicants' claims, as discussed above are not mere "obvious" (as Examiner has contended) differences but substantive recitation of structure and function coacting to achieve a new and unexpected result.

It is believed that because of the fundamental shortcomings of Gu, Examiner has cited a large number of additional references, including references cited as evidence that FIFO's were previously used as flexible storage. Applicants note that prior uses of FIFO registers were in a context different from Applicants' invention. By way of example, Applicants would like to note that the previously discussed and cited Song patent (not specifically asserted in the current Office Action) foregoes the use of a PLL and instead uses a single loop delay locked loop to receive packet (bursty) data. Column 1, lines 38-58 relied on by Examiner confirm this, as well as the fact that Song actually teaches away from Applicants' invention. Note that in Song, the FIFO is used as a coarse delay line element (CDLL) used in conjunction with a lower range fine delay

line (FDLL). The Song approach is limited to packet data, because Song delays the received data to align it to the local clock, so the timing on the delay line must be reset to the center at the beginning of each packet. Song's approach is suitable only for packet data and will not work for plesiochronous systems. Neither Song nor any other reference teaches the transmission of data with low jitter in a plesiochronous system.

In short, Applicants use a FIFO for matching the data rate (which they don't control) to the transmit rate (which they have to make as spectrally pure as possible). These are problems neither addressed nor solved by Gu, Song, Schatz, Filip, Montaz, Schmid, Rotsoll, Kirkpatrick, Wu, or any other reference. For this reason, the unique connection and coaction of elements and method steps as claimed by Applicants produce a new and unexpected result and are unobvious in the sense of 35USC103.

For the sake of completeness, it is noted that while reviewing the Wu patent, it was noticed that the closest similarity to Applicants' invention is that Wu discloses a variable delay. This function, however, is only a minor aspect of Applicants' invention.

The distinctions over Gu have been extensively explained both in this amendment and prior amendments. The Filip patent discloses a lock detector. There is no phase shifter in the Filip patent. Examiner specifically notes column 5 lines 16-62 in Filip as disclosing correlations of executions between phase detectors with a phase shifter and VCO. However, none of this so-called correlation of executions in any way suggests Applicants' invention. The Schatz patent addresses the problem of how to fill data.

Applicants have previously noted how their invention avoids the need to fill data. The Momtaz patent addresses quickly acquiring a lock on a receiver PLL by multiplexing the phase detector on the receiver between a reference clock and the received data stream. Examiner specifically relies on Column 1, lines 15-21 in Montaz, where Montaz describes the Field of the Invention related to his patent. Applicants' do not disagree with the cited portion of the Montaz patent, but respectfully point out that nothing in Montaz even remotely suggests Applicants' invention. Kirkpatrick at column 2 lines 32-44, cited by Examiner, describes a variable loop filter including a narrow band loop filter and a wide band loop filter. Applicants agree that they also have a structure

that includes a narrow band loop filter and a wide band loop filter. However, Applicants' claimed invention is in the context of a different problem and solution that neither Kirkpatrick nor any other reference purports to suggest. There is no suggestion anywhere in the prior art that such two loop filters could be advantageously used in a plesiochronous transmitter/serializer. Clark is cited for the proposition of ideas of translating analog signals into digital signals. This teaching, in no way, renders Applicants' invention obvious.

In conclusion, claims 1, 2, 8, 16 and 22 have been canceled. Claim 36 has been indicated as allowable pending only non-prior art related matters. Claims 3-7 and 9 are believed similarly allowable by Examiner as no prior art rejections have been raised with respect to these claims. Newly added claim 37 is also believed to be allowable as it depends from an allowable claim and also recites additional features of the invention. Claims 10-15, and 17-35 are believed to be allowable in view of the herein discussed amendments and rationale. Examiner is respectfully requested to telephone the undersigned if there is a question or if such would further the prosecution of this application. An early notification of allowance is earnestly solicited.

Respectfully submitted,
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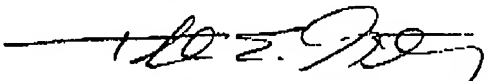

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